National Institute of Technology Silchar

(An Institute of National Importance by MHRD, Govt. of India)

Silchar, Assam – 788 010

GIAN: Global Initiative of Academic Network

An Initiative of

Ministry of Human Resource Development
Government of India

Mapping Algorithms to VLSI Architectures

Overview

Over the years, while the complexity of various applications has been growing steadily on one hand, the target computing systems on the other hand are subjected to increasingly more stringent and mutually conflicting constraints and specifications such as high throughput rate for real-time processing, less power consumption for mobile and portable systems, and less hardware requirement to achieve smaller form factors. This course will cover the methodologies for mapping algorithms to suitable architecture for achieving the desired timing performance, chip-area and energy-consumption.

The objective of this course is to introduce the concepts, methodologies, and tools necessary for mapping algorithms to architectures, which could be dedicated architectures or programmable parallel architectures. It includes the basic transformational techniques and implementation of pipelining and parallel processing. A major part of the course contains a systematic approach for mapping algorithms to possible target architectures. It also includes the design techniques for constraint-driven dedicated architectures which take care of the system constraints and requirements like processing time, power consumption, cost, and size along with the possible trade-off considerations. Apart from these, it covers a brief overview of hardware software co-design methodology and algorithm-architecture co-design followed by the fundamentals of high-level synthesis.

Participants will learn these topics through lectures and hands-on lab, tutorials, assignments and discussions on research work. Also case studies and assignments will be shared to stimulate research motivation of the participants.

Dates	**1st August 2016 to 5th August 2016**
Place & Venue	**Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Assam, India.** **Venue: Virtual Class Room, Central Computer Centre, ECE/CSE Building**
Modules to Cover	**A: Fundamental concepts, VLSI design criteria, and graphical representation of algorithms (1st Aug)** **B: Transformational techniques for architecture designs systems (2nd Aug)** **C: Parallel processing, pipelining, and design-space exploration (3rd Aug)** **D: Methodology for mapping algorithms to VLSI array architectures (4th Aug)** **E: Hardware-software co-design and high-level synthesis (5th Aug)**
Who can Participate?	• UG, PG students and research scholars of all areas of engineering and applied sciences. • Researchers from R&D laboratories working in the field of VLSI Design and Architecture (but not limited). • Faculty from reputed academic and other technical institutions. **NUMBER OF PARTICIPANTS FOR THE COURSE IS LIMITED TO FIFTY (50)**
Registration Fees of Participants	**Industry/ Research Organizations: INR 10,000** **Academic Institutions (Faculty) : INR 5,000** **Academic Institutions (Students) : INR 1,000** The above fees include registration kit, instructional materials, computer usage for tutorials and assignments, 24Hr free internet facility and refreshments etc. *The outside participants may be provided twin shared accommodation on self-payment basis subject to availability in institute guest house.* • Registration will be accepted as first come first serve basis and limited to 50. • Confirmation of participation will be intimated over Email. • Due date of Registration: **25th July 2016**
Benefits	• Participants can earn extra credit and exposure by attending GIAN expert lectures from Professor of NTU Singapore. • Opportunity to learn applications of VLSI algorithms of architectures. • Opportunity for participant to formulate research problem with the expert. • Opportunity to establish research links with the faculties from Singapore. • Opportunity to solve hands on problems in algorithms of VLSI architectures.

Foreign Faculty

Prof. P. K. Meher received the B.Sc. (Honours) and M.Sc. degrees in Physics, and Ph.D. degree in Science from Sambalpur University, India, in 1976, 1978 and 1996, respectively. Currently, he is a Senior Research Scientist with Nanyang Technological University, Singapore. For a short spell he was Professor of Computer and System Sciences in Visva Bharati University, Shantiniketan. Previously, he was a Professor of Computer Applications with Utkal University, India, from 1997 to 2002, and a Reader in Electronics with Berhampur University, India, from 1993 to 1997. His research interest includes design of dedicated and reconfigurable architectures for algorithms pertaining to signal processing, image and video processing, communication, bio-informatics, and intelligent computing. He has published nearly 230 technical papers, which includes nearly 70 papers in IEEE Transactions and nearly 30 papers in highly reputed journals like Electronics Letters and other IET/IEE Proceedings, Circuits, Systems & Signal Processing (Springer), Computers & Electrical Engineering (Elsevier), Integration, the VLSI Journal (Elsevier), Signal Processing (Elsevier), and EURASIP Journal on Advances in Signal Processing., in the area of Signal Processing, Circuits and Systems and VLSI. Dr. Meher has served as a speaker for the Distinguished Lecturer Program (DLP) of IEEE Circuits Systems Society during 2011 and 2012 and Associate Editor of the IEEE Transactions on Circuits and Systems-II: Express Briefs during 2008 to 2011, Associate Editor for IEEE Transactions on Circuits and Systems-I: Regular Papers during 2012-2013, and Associate Editor for the IEEE Transactions on Very Large Scale Integration Systems. Currently he is an Associate Editor of Integration, the VLSI Journal, and Journal of Circuits, Systems & Signal Processing. Dr. Meher is a Fellow of the Institution of Electronics and Telecommunication Engineers, India. He was the recipient of the Samanta Chandrasekhar Award for excellence in research in engineering and technology for 1999. He has received the 2013 Sydney R. Parker Best Paper Award in the area of Signal Processing, and the 2013 M. N. S. Swamy Award for the best paper of the Journal of Circuits, Systems, and Signal Processing.

Foreign Faculty

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Host Faculty

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Host Faculty

Dr. T. R. Lenka is Assistant Professor in Department of Electronics and Communication Engineering, NIT Silchar, Assam. He received B.E. degree in Electronics and Communication Engineering from the National Institute of Science and Technology, Berhampur in 2000, M.Tech degree in VLSI Design from Uttar Pradesh Technical University, Lucknow in 2007 and Ph.D. degree in Electronics Engineering from Sambalpur University, Odisha in 2012. His research interest include VLSI Design, Nanoelectronics, Growth and Characterization of Nanowires and Thin films, Modeling & Simulation of III-V based-HEMT/MODFET and Junctionless Nanowire Transistor (JNT). He is Senior Member of IEEE-EDS/SSCS.

Tentative Programme Schedule

1st August 2016 - 5th August 2016

Venue: Virtual Class Room, Central Computer Centre, ECE/CSE Building

Date	Forenoon 9:00-12:30 Noon	Afternoon 2:00-5:00 PM
01/08/2016 Monday	Lectures on Mapping Algorithms to VLSI Architectures	Hands on Laboratory/Discussions on research work
02/08/2016 Tuesday	Lectures on Mapping Algorithms to VLSI Architectures	Hands on Laboratory/Discussions on research work
03/08/2016 Wednesday	Lectures on Mapping Algorithms to VLSI Architectures	Hands on Laboratory/Discussions on research work
04/08/2016 Thursday	Lectures on Mapping Algorithms to VLSI Architectures	Hands on Laboratory/Discussions on research work
05/08/2016 Friday	Lectures on Mapping Algorithms to VLSI Architectures	Hands on Laboratory/Discussions on research work