National Institute of Technology Silchar

(An Institute of National Importance by MHRD, Govt. of India)

Silchar, Assam – 788 010

GIAN: Global Initiative of Academic Networks

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Ministry of Human Resource Development
Government of India

Nanoelectronics Challenges for Internet of Things

Overview

Current trends in Internet of Things (IoT) require the convergence of Nano electronics, Nanotechnology and Information Technology. Continued scaling of the transistor and shrinking of the physical feature sizes of the digital functionalities (logic and memory storage) in order to improve density (cost per function reduction), performance (high speed) and devices with extremely low power consumption is still following Moore's Law (More Moore). However, scaling limit is driving the incorporation of different Nano devices into Nano systems with functionalities that do not necessarily scale according to "Moore's Law", but provide additional value in different ways (more than Moore).

Low power requirements by the International Technology Roadmap for Semiconductors (ITRS) dictate integration of high-k metal gates and novel devices such as FINFETs in CMOS technologies. To attend the current trend in device scaling for sub-16 nm CMOS technology (More Moore) EOT scaling of gate dielectric beyond 0.7 nm will be required. It is therefore important to get exposed to the current trend in chip fabrication, device structures and fabrication (gate stack design and fabrication), device and circuit relationship and design, reliability of new devices and processes. Understanding power reduction and different techniques is also a key requirement. Various atomic layer deposition (ALD) methods of HfO_2-based high-k gate dielectrics are currently underway to enhance the dielectric constant and reliability in order to meet the above requirements. In this course various new technologies like cyclic deposition of ALD $Hf_{1-x}Zr_xO_2$ samples with x=0, 0.31, 0.8 is discussed where the dielectrics were exposed to intermediate slot plane antenna (SPA) Ar plasma (DSDS). In addition, Al percentage and distribution in HfO_2 will be discussed when $HfAlO_x$ and HfO_2 are deposited by ALD in a layered structure. To further enhance the device performance, high mobility channel materials with high-k dielectrics are currently being integrated. Substrates like Ge and GaAs are being considered for their high electron mobility.

Electrical performance in these devices depends on the high-k deposition process, precise selection of deposition parameters, predeposition surface treatments and subsequent annealing temperatures. This course will outline some of the recent developments of EOT scaling of high-k gate dielectrics on silicon and the challenges of high-k on high mobility substrates.

Dates	**5th - 9th JANUARY 2017**
Place & Venue	**Department of Electronics and Communication Engineering,** **National Institute of Technology Silchar, Assam, India.** Venue: Virtual Class Room, Central Computer Centre, ECE/CSE Building
Modules to Cover	**DAY 1: Convergence of Nanoelectronics, Nanotechnology and Information Technology for Internet of Things (IoTs). Low Power requirement in nanoscale CMOS Devices and introduction of high dielectric constant materials.** **DAY 2: Si-SiO_2 Interface to High-k-Ge/III-V Interface. Role of Hydrogen in Dielectrics for Electronic and Optoelectronic Devices.** **DAY 3: Breakdown principles and Complexity of Gate dielectrics breakdown with new technologies. Reliability of Silicon CMOS with SiO_2 and high-k gate dielectrics.** **DAY 4: Impact of atomic layer deposition (ALD) methods of HfO_2-based high-k gate dielectrics. Characterization issues in nanoscale CMOS devices.** **DAY 5: New electronic and optoelectronic devices for Nano systems. Circuit applications, circuit speeds and high performance circuits.**
Who can Participate?	• UG, PG students and research scholars of all areas of engineering and applied sciences. • Researchers from R&D laboratories working in the field of Nanoelectronics. • Faculty from reputed academic and other technical institutions. **NUMBER OF PARTICIPANTS FOR THE COURSE IS LIMITED TO FIFTY (50)**
Registration Fees of Participants	**Participants from Abroad : USD 500 (Early bird: USD 400 by 30 Nov 2016)** **Industry/ Research Organizations: INR 10,000 (Early bird: INR 8000 by 30 Nov 2016)** **Academic Institutions (Faculty) : INR 5,000 (Early bird: INR 3000 by 30 Nov 2016)** **Academic Institutions (Students) : INR 1,000** **The above fee includes registration kit, instructional materials, computer usage for tutorials and**

	assignments, 24Hr free internet facility and refreshments etc. ***The outside participants may be provided twin shared accommodation on self-payment basis subject to availability in institute guest house.*** **[For more details visit**: http://www.nits.ac.in/gian/gian.php] • **Registration will be accepted as first come first serve basis and limited to 50.** • **Confirmation of participation will be intimated over registered Email.** • **Due date of Registration: 15th Dec 2016**
Benefits	• Participants can earn extra credit and exposure by attending GIAN expert lectures from Professor of NJIT, New Jersey, USA. • Opportunity to learn applications of Nanoelectronics in data science. • Opportunity for participants to formulate research problem with the expert. • Opportunity to establish research links with the faculties from USA. • Opportunity to solve practical problems in device and circuit fabrication technologies.

Foreign Faculty

Prof. Durgamadhab Misra is a Professor in the Department of Electrical and Computer Engineering, New Jersey Institute of Technology, Newark, USA. He served as the Director of Microelectronics Research Center at NJIT. In 1997, he worked on plasma charging damage to CMOS devices at the VLSI Research Department, Bell Laboratories, Lucent Technologies. His current research interests are in the areas of nanoelectronic/optoelectronic devices and circuits; especially in the area of nanometer CMOS gate stacks and device reliability. Prof. Misra received several research awards from the National Science Foundation, NASA, State of New Jersey and various Industries. He received the IEEE Regional Activities Board's International Leadership Award. He is currently a Distinguished Lecturer of IEEE Electron Devices Society (EDS) and serving in the IEE EDS Board of Governors. He served as the EDS SRC Chair for North America East (Regions 1, 2, 3, and 7). He has organized many IEEE International Conferences on Solid-State Science and Technology field and at the Technical Meetings of the Electrochemical Society as General Chair, Program Chair and Track Chair, Technical Program Committee member. He is a Fellow of the Electrochemical Society (ECS) and served in the ECS Board as a Board Member (2008-10). He received the Thomas Collinan Award from the Dielectric Science & Technology Division of ECS. He is also the winner of the Electronic and Photonic Division Award from ECS. He edited and co-edited more than 40 books and conference proceedings in his field of research. He has published more than 85 technical articles in peer reviewed Journals and more than 160 articles in International Conference proceedings including 75 Invited Talks. He has graduated 15 PhD students and 35 MS students. He received the M.S. and Ph.D. degrees in electrical engineering from the University of Waterloo, Waterloo, ON, Canada, in 1985 and 1988, respectively. A detailed CV of Prof. Misra can be found at:

https://web.njit.edu/~dmisra/lab/pdf/FullCV_Misra_06_2015.pdf

Foreign Faculty

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Host Faculty

Dr. T. R. Lenka is Assistant Professor in Department of Electronics and Communication Engineering, NIT Silchar, Assam. He received B.E. degree in Electronics and Communication Engineering from the National Institute of Science and Technology, Berhampur, M.Tech degree in VLSI Design from Uttar Pradesh Technical University, Lucknow and Ph.D. degree in Electronics Engineering from Sambalpur University, Odisha. His research interest include VLSI Design, Nanoelectronics, Growth and Characterization of Nanowires and Thin films, Modeling & Simulation of III-V based-HEMT/MODFET and Junctionless Nanowire Transistor (JNT) and III-V Comound Semiconductor Nanowires for solar Cell. He has gaduated 2 PhD students and 15 M.Tech students. He has published 40 research papers in peer reviewed Journals and 25 research articles in Internnational Conference Proceedings. He is Senior Member of IEEE-EDS/SSCS and Member of Institution of Engineers (IE).

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Course ID: 161031D02

Tentative Programme Schedule

05th - 09th Jan 2017

Venue: Virtual Class Room, Central Computer Centre, ECE/CSE Building

Date	Forenoon 10:00 - 12:00 Noon	Evening 3:00-5:00 PM
05/01/2017 Thursday	(**Inauguration @ 09:30 AM**) Lectures on: Convergence of Nanoelectronics, Nanotechnology and Information Technology for Internet of Things (IoTs)	Lectures on : Low Power requirement in nanoscale CMOS Devices and introduction of high dielectric constant materials.
06/01/2017 Friday	Lectures on : Si-SiO_2 Interface to High-k-Ge/III-V Interface	Lectures on : Role of Hydrogen in Dielectrics for Electronics and Optoelectronics Device
07/01/2017 Saturday	Lectures on : Breakdown principles and Complexity of Gate dielectrics breakdown with new technologies.	Lectures on : Reliability of Silicon CMOS with SiO_2 and high-k gate dielectrics.
08/01/2017 Sunday	Lectures on: Impact of atomic layer deposition (ALD) methods of HfO_2-based high-k gate dielectrics	Lectures on : Characterization issues in nanoscale CMOS devices.
09/01/2017 Monday	Lectures on : New electronic and optoelectronic devices for Nano systems.	Lectures on : • Circuit applications, circuit speeds and high performance circuits • How to innovate as a researcher? **Valedictory Session @ 5 PM**

Note: The participants are required to 1st register in the GIAN Portal http://www.gian.iitkgp.ac.in/ by paying the requisite one time registration fee. Then they can register for this course by filling the registration form available at http://www.nits.ac.in/gian/gian.php by paying the registration fee.